ispLSI® 2128VE

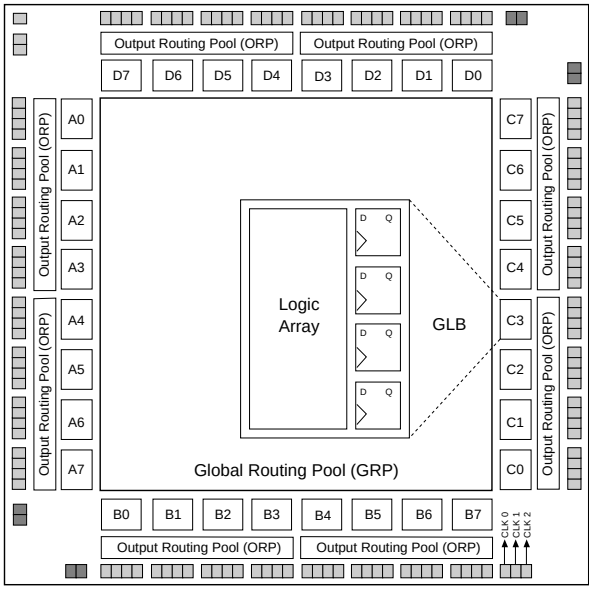
3.3V In-System Programmable SuperFAST™ High Density PLD

Lead-Free Package Options Available!

Features

- **SuperFAST HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - **6000 PLD Gates**
  - **128 and 64 I/O Pin Versions, Eight Dedicated Inputs**
  - **128 Registers**
  - **High Speed Global Interconnect**
  - **Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **Small Logic Block Size for Random Logic**
  - **100% Functional, JEDEC and Pinout Compatible with ispLSI 2128V Devices**
- **3.3V LOW VOLTAGE 2128 ARCHITECTURE**
  - **Interfaces with Standard 5V TTL Devices**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **fmax = 250MHz Maximum Operating Frequency**
  - **tpd = 4.0ns Propagation Delay**
  - **Electrically Erasable and Reprogrammable**
  - **Non-Volatile**
  - **100% Tested at Time of Manufacture**
  - **Unused Product Term Shutdown Saves Power**
- **IN-SYSTEM PROGRAMMABLE**
  - **3.3V In-System Programmability (ISP™) Using Boundary Scan Test Access Port (TAP)**
  - **Open-Drain Output Option for Flexible Bus Interface Capability, Allowing Easy Implementation of Wired-OR Bus Arbitration Logic**
  - **Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality**
  - **Reprogram Soldered Devices for Faster Prototyping**
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE**
- **THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FPGAS**
  - **Enhanced Pin Locking Capability**
  - **Three Dedicated Clock Input Pins**
  - **Synchronous and Asynchronous Clocks**
  - **Programmable Output Slew Rate Control**
  - **Flexible Pin Placement**
  - **Optimized Global Routing Pool Provides Global Interconnectivity**
- **LEAD-FREE PACKAGE OPTIONS**

Functional Block Diagram*



*128 I/O Version Shown

0139A/2128VE

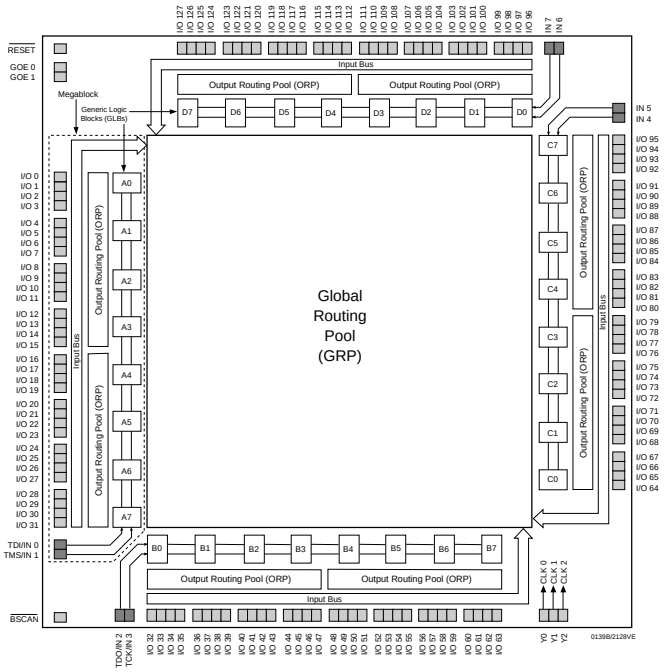
Description

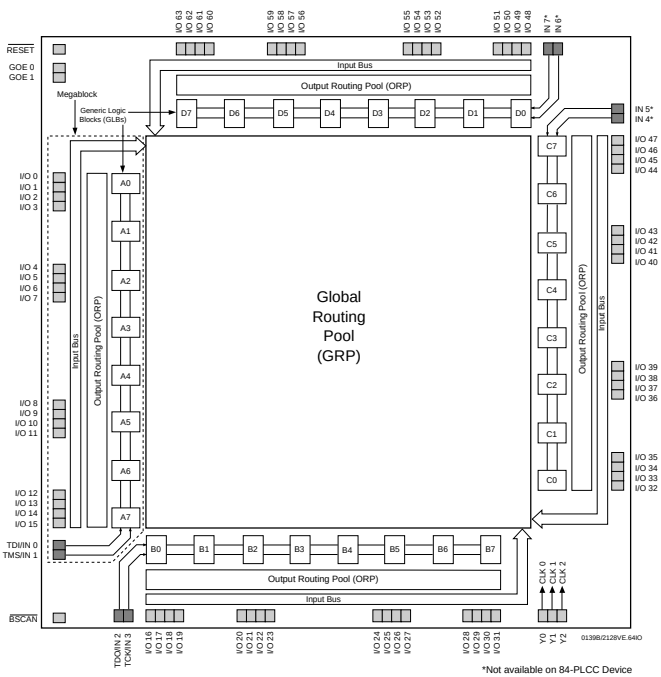
The ispLSI 2128VE is a High Density Programmable Logic Device available in 128 and 64 I/O-pin versions. The device contains 128 Registers, eight Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2128VE features in-system programmability through the Boundary Scan Test Access Port (TAP) and is 100% IEEE 1149.1 Boundary Scan Testable. The ispLSI 2128VE offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 2128VE device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (see Figure 1). There are a total of 32 GLBs in the ispLSI 2128VE device. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 2128VE Functional Block Diagram (128-I/O and 64-I/O Versions)





The 128-I/O 2128VE contains 128 I/O cells, while the 64-I/O version contains 64 I/O cells. Each I/O cell is directly connected to an I/O pin and can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4mA or sink 8mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise. Device pins can be safely driven to 5V signal levels to support mixed-voltage systems.

Eight GLBs, 32 or 16 I/O cells, two dedicated inputs and two or one ORPs are connected together to make a Megablock (see Figure 1). The outputs of the eight GLBs are connected to a set of 32 or 16 universal I/O cells by the two or one ORPs. Each ispLSI 2128VE device contains four Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2128VE device are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Programmable Open-Drain Outputs

In addition to the standard output configuration, the outputs of the ispLSI 2128VE are individually programmable, either as a standard totem-pole output or an open-drain output. The totem-pole output drives the specified Voh and Vol levels, whereas the open-drain output drives only the specified Vol. The Voh level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by a programmable fuse. The default configuration when the device is in bulk erased state is totem-pole configuration. The open-drain/totem-pole option is selectable through the Lattice software tools.

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +5.4V

Input Voltage Applied ..... -0.5 to +5.6V

Off-State Output Voltage Applied ..... -0.5 to +5.6V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	3.0	3.6	V
		Industrial	T_A = -40°C to + 85°C	3.0	3.6	V
V_{IL}	Input Low Voltage			V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage			2.0	5.25	V

Table 2-0005/2128VE

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	Dedicated Input Capacitance	8	pf	V_{CC} = 3.3V, V_{IN} = 0.0V
C_2	I/O Capacitance	6	pf	V_{CC} = 3.3V, $V_{I/O}$ = 0.0V
C_3	Clock and Global Output Enable Capacitance	10	pf	V_{CC} = 3.3V, V_Y = 0.0V

Table 2-0006/2128VE

Erase Reprogram Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Erase/Reprogram Cycles	10,000	–	Cycles

Table 2-0008/2128VE

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 1.5ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

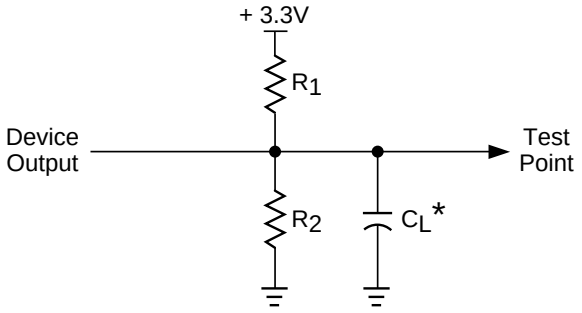
Table 2 - 0003/2128VE

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		316Ω	348Ω	35pF
B	Active High	∞	348Ω	35pF
	Active Low	316Ω	348Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	348Ω	5pF
	Active Low to Z at V_{OL} +0.5V	316Ω	348Ω	5pF

Table 2-0004/2128VE

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A/2128VE

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	(V_{CC} - 0.2)V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
		V_{CC} ≤ V_{IN} ≤ 5.25V	–	–	10	µA
I_{IL-isp}	$\overline{BSCAN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 3.3V, V_{OUT} = 0.5V	–	–	-100	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{CLOCK} = 1 MHz	–	195	–	mA

Table 2-0007/2128VE

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC} .

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST[3] COND.	#	DESCRIPTION[1]	-250		-180		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	4.0	–	5.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	6.0	–	7.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[2]	250	–	180	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{tsu2 + tco1}\right)$	158	–	125	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	277	–	200	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	2.5	–	3.5	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	3.0	–	3.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	3.3	–	4.5	–	ns
t_{co2}	A	10	GLB Reg. Clock to Output Delay	–	3.7	–	4.5	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	–	6.0	–	7.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	3.5	–	4.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	6.0	–	10.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	6.0	–	10.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	4.0	–	5.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	4.0	–	5.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	1.8	–	2.5	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	1.8	–	2.5	–	ns

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030A/2128VE
v.1.0

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[3]	#	DESCRIPTION[1]	-135		-100		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	—	7.5	—	10.0	ns
t_{pd2}	A	2	Data Propagation Delay	—	10.0	—	13.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[2]	135	—	100	—	MHz
f_{max} (Ext.)	—	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	100	—	77	—	MHz
f_{max} (Tog.)	—	5	Clock Frequency, Max. Toggle	143	—	100	—	MHz
t_{su1}	—	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	5.0	—	6.5	—	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	—	4.0	—	5.0	ns
t_{h1}	—	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	—	0.0	—	ns
t_{su2}	—	9	GLB Reg. Setup Time before Clock	6.0	—	8.0	—	ns
t_{co2}	A	10	GLB Reg. Clock to Output Delay	—	5.0	—	6.0	ns
t_{h2}	—	11	GLB Reg. Hold Time after Clock	0.0	—	0.0	—	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay, ORP Bypass	—	9.0	—	12.5	ns
t_{rw1}	—	13	Ext. Reset Pulse Duration	5.0	—	6.5	—	ns
t_{ptoeen}	B	14	Input to Output Enable	—	12.0	—	15.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	—	12.0	—	15.0	ns
t_{goeen}	B	16	Global OE Output Enable	—	7.0	—	9.0	ns
t_{goedis}	C	17	Global OE Output Disable	—	7.0	—	9.0	ns
t_{wh}	—	18	External Synchronous Clock Pulse Duration, High	3.5	—	5.0	—	ns
t_{wl}	—	19	External Synchronous Clock Pulse Duration, Low	3.5	—	5.0	—	ns

1. Unless noted otherwise, all parameters use a GRP load of four, 20 PTXOR path, ORP and Y0 clock.
2. Standard 16-bit counter using GRP feedback.
3. Reference Switching Test Conditions section.

Table 2-0030B/2128VE
v.1.0

Internal Timing Parameters[1]

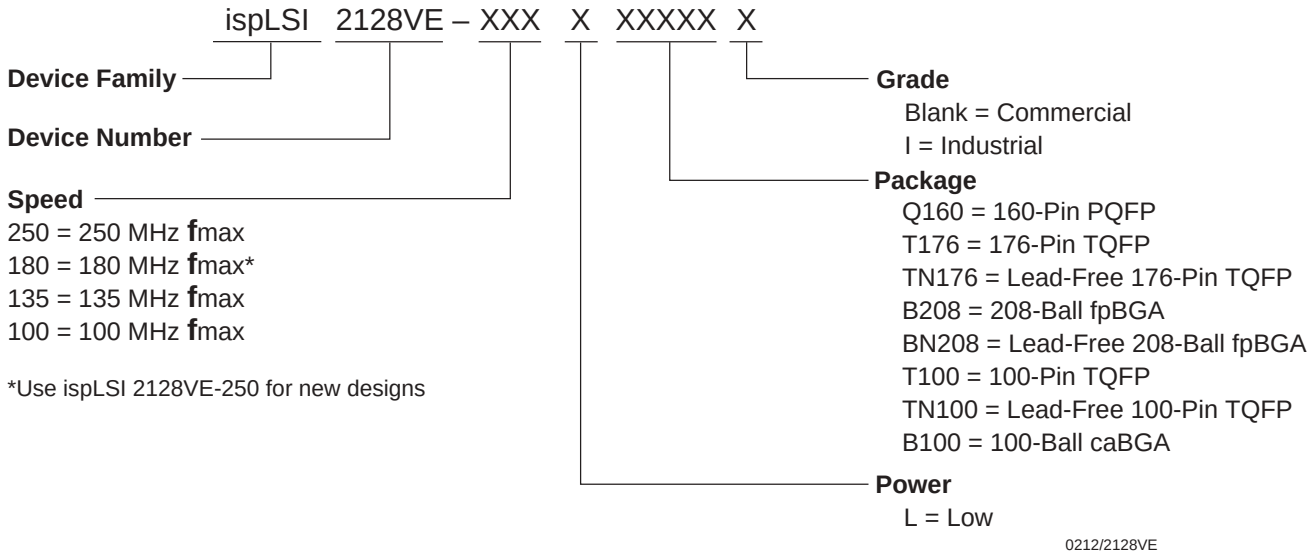
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-135		-100		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	—	0.5	—	0.7	ns
t_{din}	21	Dedicated Input Delay	—	1.7	—	2.5	ns
GRP							
t_{grp}	22	GRP Delay	—	1.2	—	1.8	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay (Combinatorial)	—	3.7	—	5.2	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay (Registered)	—	3.7	—	4.7	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	—	4.7	—	6.2	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	—	4.7	—	6.2	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	—	4.7	—	6.2	ns
t_{gbp}	28	GLB Register Bypass Delay	—	0.5	—	1.0	ns
t_{gsu}	29	GLB Register Setup Time before Clock	1.2	—	1.7	—	ns
t_{gh}	30	GLB Register Hold Time after Clock	3.8	—	4.8	—	ns
t_{gco}	31	GLB Register Clock to Output Delay	—	0.3	—	0.3	ns
t_{gro}	32	GLB Register Reset to Output Delay	—	1.1	—	3.1	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	—	6.1	—	7.1	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	—	6.9	—	9.1	ns
t_{ptck}	35	GLB Product Term Clock Delay	1.6	4.6	2.6	5.6	ns
ORP							
t_{orp}	36	ORP Delay	—	1.5	—	1.7	ns
t_{orpbp}	37	ORP Bypass Delay	—	0.5	—	0.7	ns
Outputs							
t_{ob}	38	Output Buffer Delay	—	1.6	—	1.6	ns
t_{sl}	39	Output Slew Limited Delay Adder	—	2.0	—	2.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	—	3.4	—	3.4	ns
t_{odis}	41	I/O Cell OE to Output Disabled	—	3.4	—	3.4	ns
t_{goe}	42	Global Output Enable	—	3.6	—	5.6	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	1.6	1.6	2.4	2.4	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	1.8	1.8	2.6	2.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	—	5.8	—	7.1	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Table 2-0036B/2128VE
v.1.0

Part Number Description



0212/2128VE

ispLSI 2128VE Ordering Information

Conventional Packaging

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	250	4.0	128	ispLSI 2128VE-250LT176	176-Pin TQFP
	250	4.0	128	ispLSI 2128VE-250LQ160	160-Pin PQFP
	250	4.0	128	ispLSI 2128VE-250LB208	208-Ball fpBGA
	250	4.0	64	ispLSI 2128VE-250LT100	100-Pin TQFP
	250	4.0	64	ispLSI 2128VE-250LB100	100-Ball caBGA
	180	5.0	128	ispLSI 2128VE-180LT176*	176-Pin TQFP
	180	5.0	128	ispLSI 2128VE-180LQ160*	160-Pin PQFP
	180	5.0	128	ispLSI 2128VE-180LB208*	208-Ball fpBGA
	180	5.0	64	ispLSI 2128VE-180LT100*	100-Pin TQFP
	180	5.0	64	ispLSI 2128VE-180LB100*	100-Ball caBGA
	135	7.5	128	ispLSI 2128VE-135LT176	176-Pin TQFP
	135	7.5	128	ispLSI 2128VE-135LQ160	160-Pin PQFP
	135	7.5	128	ispLSI 2128VE-135LB208	208-Ball fpBGA
	135	7.5	64	ispLSI 2128VE-135LT100	100-Pin TQFP
	135	7.5	64	ispLSI 2128VE-135LB100	100-Ball caBGA
	100	10	128	ispLSI 2128VE-100LT176	176-Pin TQFP
	100	10	128	ispLSI 2128VE-100LQ160	160-Pin PQFP
	100	10	128	ispLSI 2128VE-100LB208	208-Ball fpBGA
	100	10	64	ispLSI 2128VE-100LT100	100-Pin TQFP
	100	10	64	ispLSI 2128VE-100LB100	100-Ball caBGA

*Use ispLSI 2128VE-250 for new designs

Table 2-0041A/2128VE

ispLSI 2128VE Ordering Information (Cont.)

Conventional Packaging (Cont.)

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	135	7.5	64	ispLSI 2128VE-135LT100I	100-Pin TQFP
	135	7.5	128	ispLSI 2128VE-135LT176I	176-Pin TQFP

Table 2-0041B/2128VE

Lead-Free Packaging

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	250	4.0	128	ispLSI 2128VE-250LTN176	Lead-Free 176-Pin TQFP
	250	4.0	128	ispLSI 2128VE-250LBN208	Lead-Free 208-Ball fpBGA
	250	4.0	64	ispLSI 2128VE-250LTN100	Lead-Free 100-Pin TQFP
	135	7.5	128	ispLSI 2128VE-135LTN176	Lead-Free 176-Pin TQFP
	135	7.5	128	ispLSI 2128VE-135LBN208	Lead-Free 208-Ball fpBGA
	135	7.5	64	ispLSI 2128VE-135LTN100	Lead-Free 100-Pin TQFP
	100	10	128	ispLSI 2128VE-100LTN176	Lead-Free 176-Pin TQFP
	100	10	128	ispLSI 2128VE-100LBN208	Lead-Free 208-Ball fpBGA
	100	10	64	ispLSI 2128VE-100LTN100	Lead-Free 100-Pin TQFP

INDUSTRIAL

FAMILY	fmax (MHz)	tpd (ns)	I/Os	ORDERING NUMBER	PACKAGE
ispLSI	135	7.5	128	ispLSI 2128VE-135LTN176I	Lead-Free 176-Pin TQFP
	135	7.5	64	ispLSI 2128VE-135LTN100I	Lead-Free 100-Pin TQFP